SEE and TID of Emerging Non-Volatile Memories

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Abstract – **We report on the SEE and TID tests of higher density flash memories. Stand-by currents and functionality tests were used to characterize the response of radiation effects. Single Event Functional Interrupt (SEFI) errors were observed indicating upsets from complex control circuitry.**

I. INTRODUCTION

As non-volatile memories become the memory standard of today digital audio, video and camera equipment, semiconductor manufacturers are struggling to supply low-cost high-density flash memories to fulfill the increasing demand [1]. Besides consumer electronics applications, flash memories have been used in solid-state recorders in space mission systems. Previous solid-state recorders were designed around reliable, robust and radiation-hardened dynamic random access memories but current recorders for space missions are being built with flash memory devices. Most critical systems of space instruments require redundancy to ensure backup coverage. Redundancy can be built around multi-chip-module (MCM), which contains duplicates of one die installed in a single package. MCM components that are packed with two or more flash memory die of a similar type can backup data among themselves and then can be directed into different modes. Newer flash memories add multi-block program, multi-block erase, and multi-level storage [2].

There are two types of flash architecture: NOR and NAND. While both architectures have the same basic storage element (consisting of a control gate stacked over an insulating oxide known as a floating gate, a source, and a drain), it is the interconnection of these memory cells that distinguishes the structure. In the NOR flash memory array, the bit line logic goes to "0" if any of the memory cell transistors is "ON". In the NAND flash memory array, the bit line logic goes to "0" if all of the memory cell transistors are "ON". Both architectures require charge pump circuits in order to provide the high internal voltages that are needed for erase and write operations.

The memory cells of NAND architecture require 20 volts for writing and erasing, while cells of NOR structure need 12 volts for erase and write functions [3]. NOR flash memories use Fowler-Nordheim (F-N) tunneling to remove electrons from the floating gate during erasure and inject hot electrons to the floating gate during writing. The NAND type structure inherited more uniform charge transfer between its floating gate and its body since only F-N tunneling is activated for both erasing and writing. The NOR memory structure has relatively fast random read speed, but it has slow erase and write speeds compared to its NAND counterpart. The NOR memory cells wear out faster due to the channel hot-electron (CHE) stress.

II. DEVICE DESCRIPTIONS

Both SanDisk SDTNF-512 and Toshiba TC58512FT are 3.3-volt 512-Mbits NAND flash memory devices, organized as 528 bytes x 32 pages x 4096 blocks. Operating modes include of multi-block program, multi-block erase, auto page program, auto block erase, read, status read, and reset.

The AeroFlex ACT-F2M32A has four AMD 29F016B die in one MCM package. It is a 5.0-volt 64Mbits NOR flash memory device, organized as 2M x 8-bit x 4 die. Modes of operation consist of any combination of sectors erasure, read or program data to a sector not being erased, auto die erase, and individual die reset.

Table 1: Comparison of AeroFlex, SanDisk and Toshiba devices

	No. of Blocks	Block Size (bytes)	Block Erase Time (Max)	Max. E/W Cycles	Initial Bad Blocks
AeroFlex 2Mx32	32	64K	1s (8s)	10^5	none
SanDisk 64Mx8	4096	16.5K	2ms (10ms)	10^6	=< 80
Toshiba 64Mx8	4096	16.5K	2ms (10ms)	10^6	=< 80

As described in Section I, both NAND and NOR flash memory technology have internal charge pump generators to provide higher voltages than their external operating supplies, for the write and erase operations. As shown in Table 1, the SanDisk and Toshiba flash devices typically require 8 seconds to erase the whole part, but the AeroFlex MCM needs at least 32 seconds to perform the similar operation. The SanDisk and Toshiba devices operate with lower currents in all modes, up to 30mA compared to 160mA (read) and 240mA (erase/write) for the AeroFlex parts.

The total of eight de-lidded parts were used for SEE testing (3 Toshiba, 2 SanDisk and 3 AeroFlex). The total of total of eight parts were used for TID tests (3 Toshiba, 3

SanDisk, and 2 AMD 29F016B). The date code is as follows: (AeroFlex ACT-FM32A) 0044, (Toshiba TC58512FTI) 0142, (SanDisk SDTNF-512) 0151, and 9611 (AMD 29F016B). AMD parts were manufactured on 0.32µm process technology [4], while Toshiba and SanDisk parts were made with 0.16µm process technology [5].

III. Test Set-up

SEE testing was done at Texas A&M cyclotrons and the Brookhaven National Laboratory (BNL). All tests were performed at 25 degree C and in vacuum. Properties of the ions used to test AeroFlex MCM, SanDisk, and Toshiba parts are listed in Table 2 and Table 3.

Table 2: Ions (at TAM) used to test AeroFlex parts

Species	LET	Angles used
Neon	1.7	0
Argon	5.4	0, 38
Krypton	19.0	0
Xenon	37.7	0,38

Table 3: Ions used to test SanDisk and Toshiba parts at BNL

Species	LET	Angles used
Lithium	0.371	0, 60, 70,73
Fluorine	3.364	0, 45, 50, 60, 67
Silicon	7.901	0, 45, 55, 60
Chlorine	11.44	0, 45, 60

The test equipment is comprised of two PCs, a power supply, and an FPGA-based test board. One PC controls a HP6629A power supply. This allows precision voltage control and latch-up detection and protection since the PC has millisecond control over the operation of the power supply. A second, dedicated PC controls the test circuit board designed specifically to read errors and write commands/test patterns to the (device under test) DUTs. Parts are programmed with a pseudo-random pattern to mimic real data. The algorithm generates a reproducible sequence of binary states. Two patterns are used to complement each other and to ensure that all bit locations are changed states. The address of any failure and the value at that address are recorded in a file for each run. The number of address and bit failures also is recorded in a separate log file. A depiction of the setup used is shown in Figure 1.

Total dose tests were done using the JPL cobalt-60 facility at the dose rate of 25 rad(Si) per second with a series of 2 krad(Si) steps and at 25 degrees C. The devices under test (DUT) were static biased during irradiation. Electrical parametric measurements were made after each irradiation step with an Advantest test system, while functional tests were evaluated with the similar SEE setup without the vacuum chamber. Functional tests consisted of the following sequences:

1. Erase, write, and read to validate stored data
2. Irradiate
3. Read pattern to ensure data retention
4. Erase, write complement data, read to validate
5. Repeat step 2.

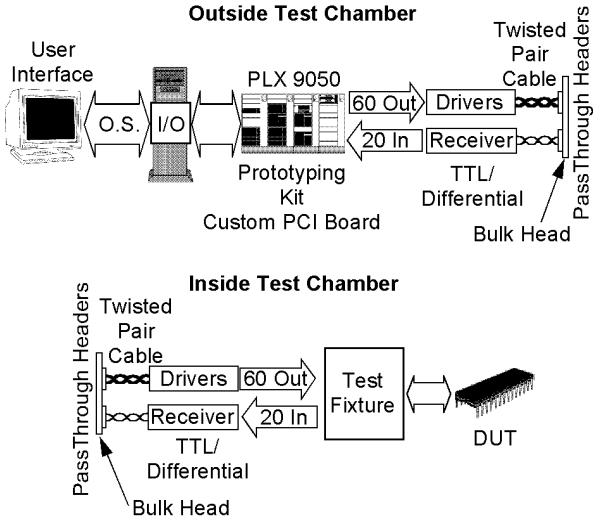

Figure 1: Test Set-Up

IV. Definitions of Errors

Read errors are defined as incorrect expected data. During a read operation, upsets occur in the state machine controller, readout buffer, and registers. Write errors are wrong data written to the device, or data are placed to wrong addresses due to the temporary malfunction of the decoder, or the whole block cannot be accessed, or the time allowed to write expires. Erase errors are created when electrons are not completely removed from floating gates, or its monitoring of complete block erase signal halts temporarily and requires many repeated passes for a successful erasure. Besides above errors, single event functional interrupt (SEFI) errors also occurred. Regular SEFIs have the following characteristics: operation suspended, higher current, happen with low LET. It is not considered a single-event latch-up (SEL). SEFI block erase errors can produce either a never-ending loop, or a partial erasure, or a failure to erase the very first few blocks. Its ready signal also can hang in the busy state forever during the block-erase process. Both read SEFI and write SEFI suspend the intended activities. Another kind of SEFI occurs after devices have been irradiated and operated in a different mode. In the case of irregular SEFI read errors, the reading sequence goes into an endless loop. Reset the power puts the device back to its normal operation. Irregular write SEFI stops the device's operation, but to initialize the device's current back to the pre-SEFI state will require recycling power and repeating the erase/write/read process. Table 4 describes the observed errors and solutions of recover SEFI locked-ups. Other studies of SEFI had been done on microprocessors, digital signal processors (DSPs), electrically erasable programmable read only memories (EEPROMs), dynamic random access memory (DRAM), and synchronous DRAMs [6][7].

Table 4: Observed SEFI errors

Error type	Description	Solutions
Block-erase SEFI	The device's ready signal never exits the busy state.	Reset power only
Partial erase SEFI	Block-erase suspends at the first address. Few blocks are erased.	Repeat the erase process.
Write SEFI	Write operation completion's status suspends.	Reset power only
Read SEFI	Sensing circuitry suspends due to charge built-up. Next read operation doesn't clear errors.	Repeat the read process or cycle power.
Irregular SEFIs	Read operation locks into endless loop. Write operation stops.	Reset power only. Reset power alone won't initialize the device's current to pre-SEFI state until re-start the erase process.

V. SEE TEST RESULTS

Three AeroFlex MCM parts (NOR technology) were tested with negligible variation among them. Figures 2, 3, and 4 were statistically fit using a model by Edmonds [6]. Three operational modes are used during irradiation: read, write and erase. Irregular SEFI happened occasionally during the post-irradiation read, following by an increase of device supply current. Figure 2 shows the measured upset cross-sections vs. LET in the dynamic read mode. No hard errors or bit erasures were seen in 10^{11} particles per centimeter. Figure 3 illustrates the measured cross-sections in the write operation. This occurs due to state machine or decoders being upset resulting in the changing of the address it is reading for validation from the address where data were written. Figure 4 shows the cross-sections vs. LET during the erase mode. The gradual cross-section curves of all three Figures 2, 3, and 4 suggest that the memory elements of the AeroFlex device have different critical charges.

The AeroFlex device showed no Single Event Latch-up at any LET. Different combinations of extreme angles and lower-energy ions did not trigger any latch up. Effective LETs of 120 MeV-cm^2 /mg were used. These tests were done at nominal conditions, at room temperature and with bias at 3.3 volts. The other two saw no SEL either.

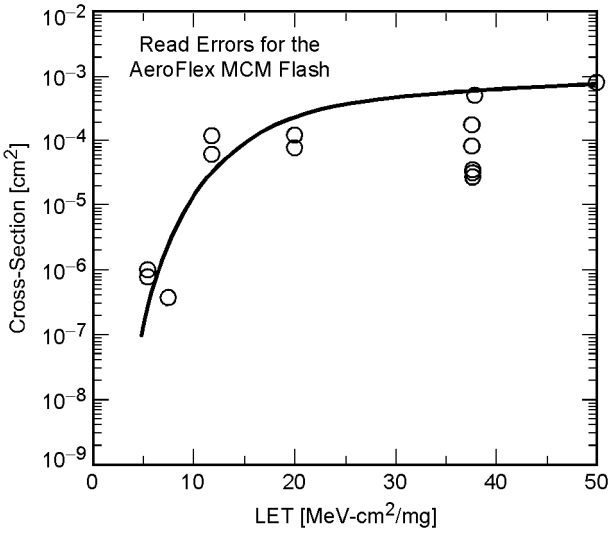

Figure 2: Cross-section of the dynamic read upsets (AeroFlex MCM)

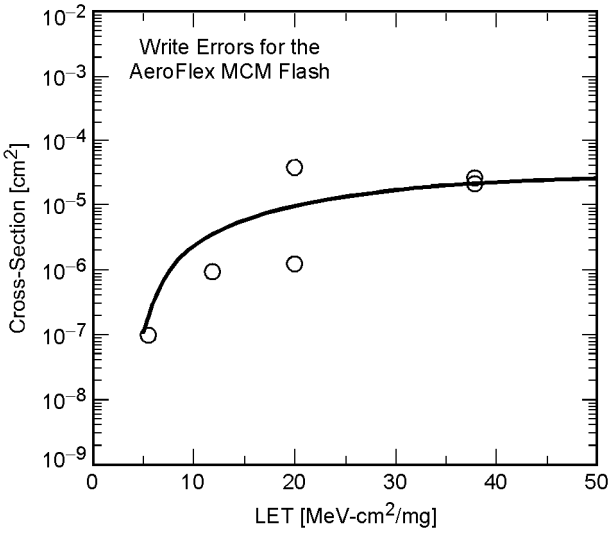

Figure 3: Cross-section of write-upsets (AeroFlex MCM)

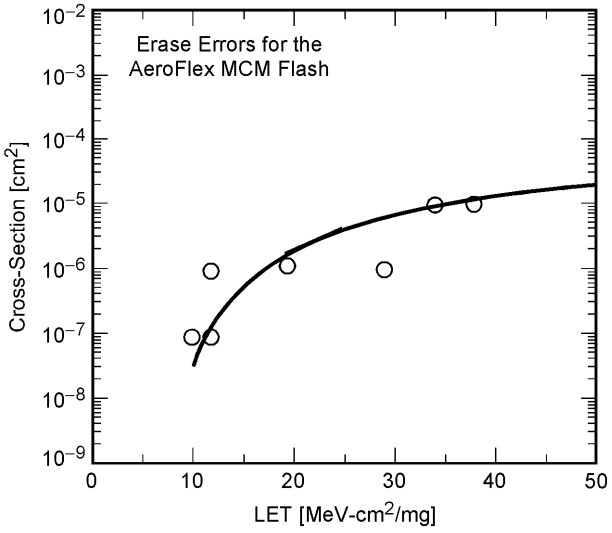

Figure 4: Cross-section of erase upsets (AeroFlex MCM)

There is no significant difference in upset threshold for both SanDisk and Toshiba parts. The SEU threshold is

approximately 4-8 MeV-cm^2 /mg for both device types. The saturation cross-section in the write mode of both parts is around 2.0E-2 cm^2. Figure 5 shows the cross-section of write upsets and SEFI of SanDisk parts. The SEFI cross-section is smaller the SEU cross-section since every SEFI is counted as one even though such event creates numerous bit errors. After locked up, the SEFI current stays at an unusual high level and will not re-initialize to idle state unless power is reset. Logic state switching in the control circuit and registers may cause internal bus contention and probably creates the sudden increase of device's current. The saturation cross-section in the read mode of SanDisk parts is 7-9 times smaller than that of the Toshiba parts as shown in Figures 6 and 8. SEU test results of three Toshiba TC58512TF de-lidded parts are shown in Figures 7 and 8.

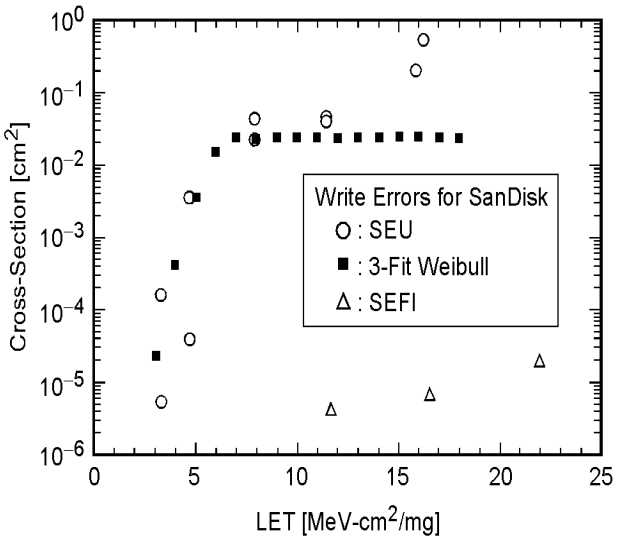

Figure 5: Cross-section of write-upsets (SanDisk)

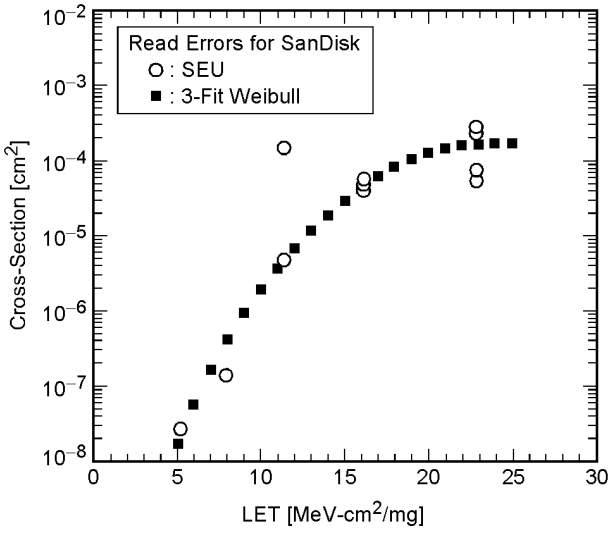

Figure 6: Cross-section of read upsets (SanDisk)

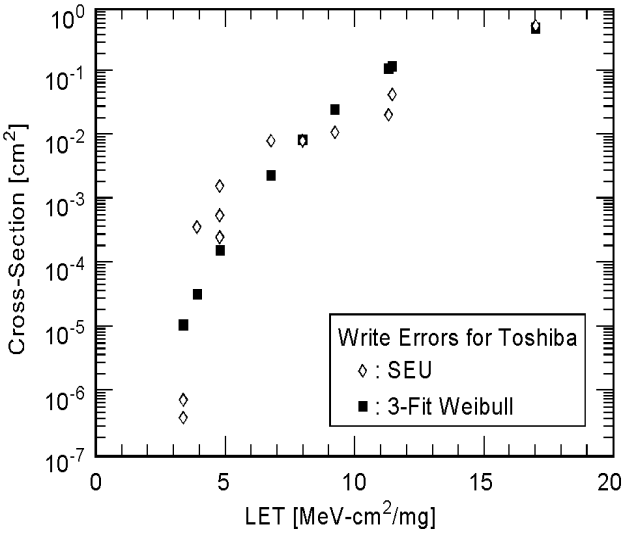

Figure 7: Cross-section of write upsets (Toshiba)

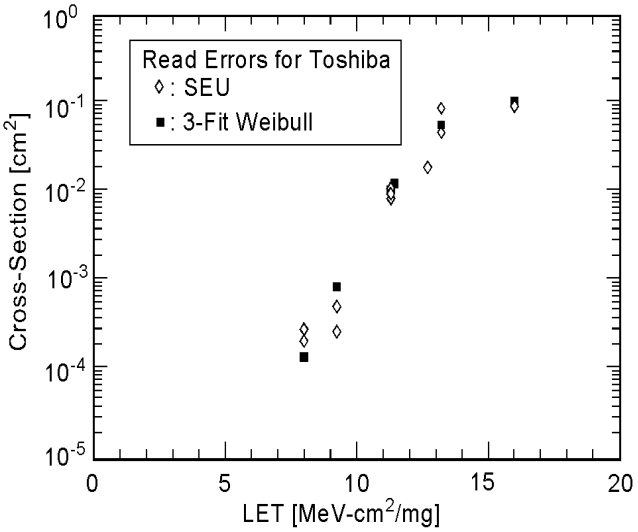

Figure 8: Cross-section of read upsets (Toshiba)

VI. TID TEST RESULTS

The stand-by currents of SanDisk devices were 12 μA at 14krad(Si) at which functional failures occurred, an increase of 5 μA from the initial measurements. After 14krad(Si), devices could be erased, but they could not be written with the complement pattern. One of three SanDisk parts recovered 24 hours later at nominal conditions, at room temperature and with bias at 3.3 volts. Two other SanDisk parts recovered after 48 hours and 72 hours respectively. All three can be erased but have few hundred thousands to more than million write errors at 16krad(Si). Figure 9 shows the TID response of three SanDisk parts.

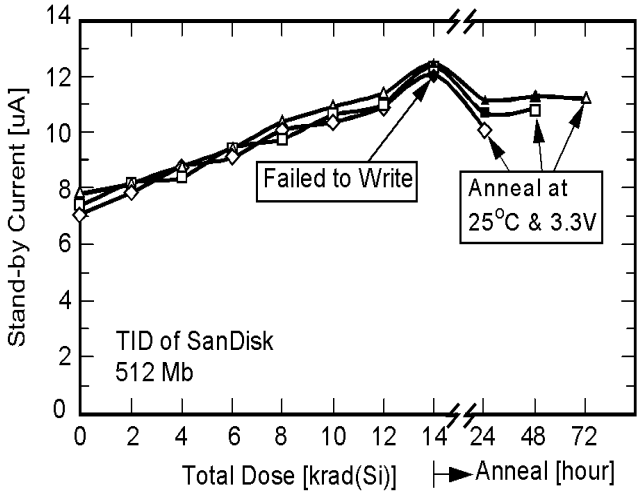

Figure 9: TID of SanDisk devices

All three Toshiba parts also failed to be written at 14krad(Si). They annealed after 24 hours later at nominal conditions. Two out of three have few hundred thousands write errors after 18krad(Si). The stand-by currents of Toshiba devices slightly increased at every 2 krad(Si) step but still were within manufacturer's specifications, 100 μA. Previous TID testing of NAND flash memory devices failed to erase at 8 krad(Si) and could not recover even at elevated temperature, 100 degrees C [7]. Figure 10 displays the TID response of Toshiba parts.

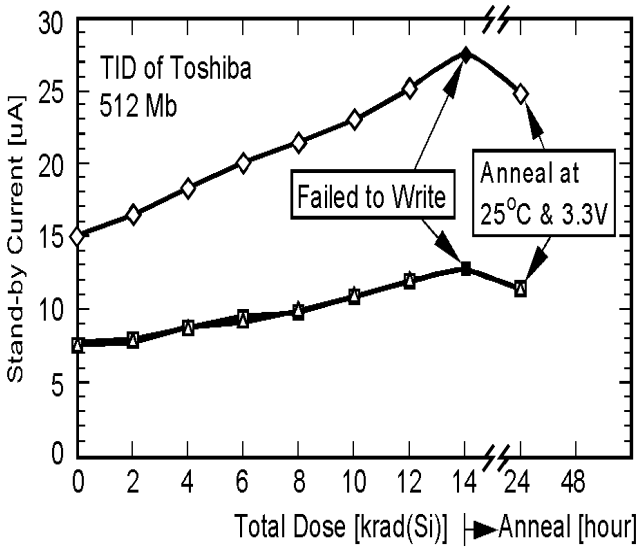

Figure 10: TID of Toshiba devices

The AeroFlex, two AMD29F016B parts, was evaluated in the similar setup as described in section III. The AMD parts failed to erase after 8 krad(Si) . The stand-by current went from less than 1 μA at the start of the test to 744 μA at 8 krad(Si), far more than the manufacturer's specifications of 5 μA. This implied that the oxide thickness of AeroFlex die is larger than those of the SanDisk and Toshiba devices. Figure 11 shows the total dose test results for the AeroFlex parts.

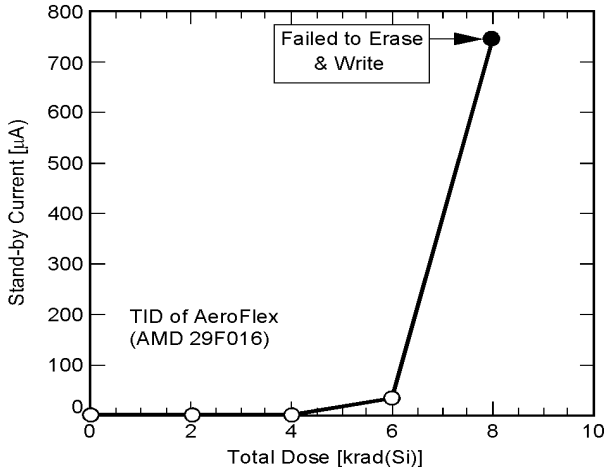

Figure 11: TID of AeroFlex MCM

VII. Conclusions

The SanDisk and Toshiba parts have better TID responses than previous, less density NAND type memories. Both still can be erased after 18krad(Si) compared to the total failure of erase function from earlier NAND flash memories after only 8krad(Si). Based on the TID test data of SanDisk and Toshiba parts, future studies need to add the write problem to the current issue of erase failures. AeroFlex's TID performance is degraded also at 8krad(Si). There is no significant difference in SEU threshold among three devices. SanDisk and Toshiba parts do not experience the post-irradiation SEFI in contrast to several AeroFlex irregular SEFIs. A future modified test method must be devised to reset the SEFI lock-up instantly, without user's intervention, to record an accurate number of SEFI.

Acknowledgment

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